Euso Front End ASIC

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on behalf of the Genova group:

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Talk overview

- Motivations, constraints and requirements
- Analog Sections design
- Digital Sections design
- The “prototype 0” design
- Phase A plans

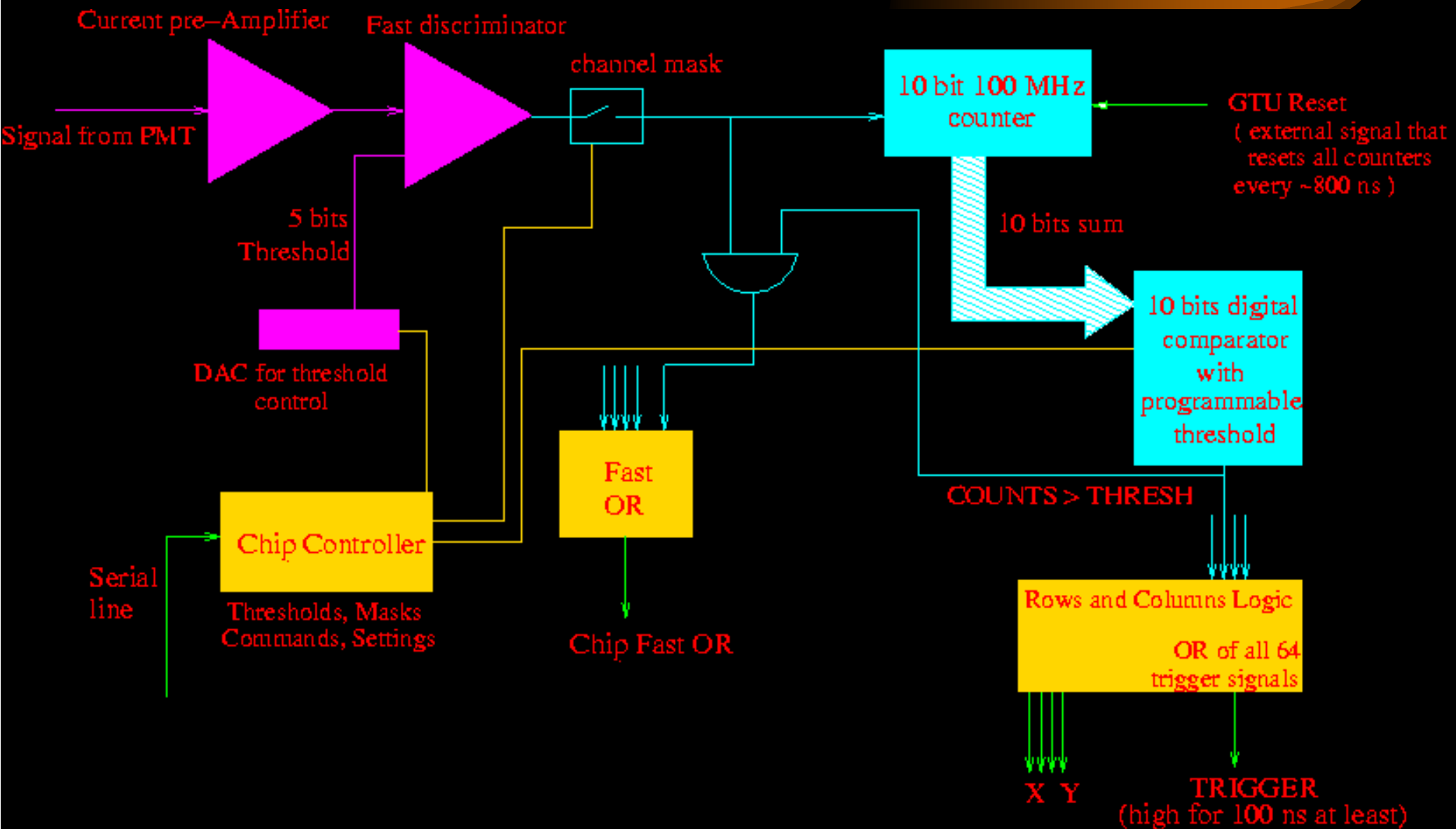
Front End functions

- The EUSO front end is needed to:
  - Pre-Amplify MAPMT signals (charge ≈5 10^5 e^-, in ≈5 ns)
  - Discriminate these signals with a programmable threshold (much lower than 1 photoelectron signal)
  - Count single photons during externally controlled time periods (GTUs, ~ 1 μs)
  - Mask noisy or bad channels
  - Provide information for the trigger system (counter thresholds, rows and columns logic)
  - Accept commands and setup parameters from a serial line

Constraints and Requirements

- Critical features are (optimal trade-offs to be identified in Phase A)
  - Optimal gain and input impedance to match the Photon Detector signal.
  - Double hit resolution **~10-15 ns**
  - Time information with precision ~ 10 ns would be nice.
  - Power Consumption must be low. Front end should eat **~ 1 mW per ch.**
  - Option: Storing capability well above a full EAS event (~100 μs)
  - Option: Trigger capabilities to improve trigger efficiency and decrease the energy threshold.

Base block diagram

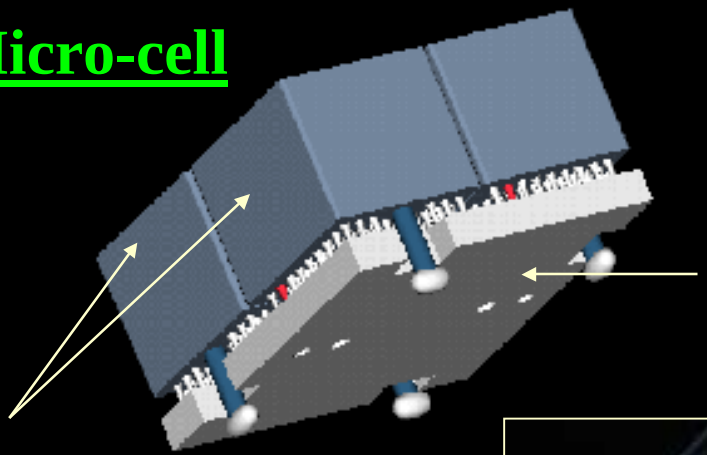


Project for a FE Custom Chip

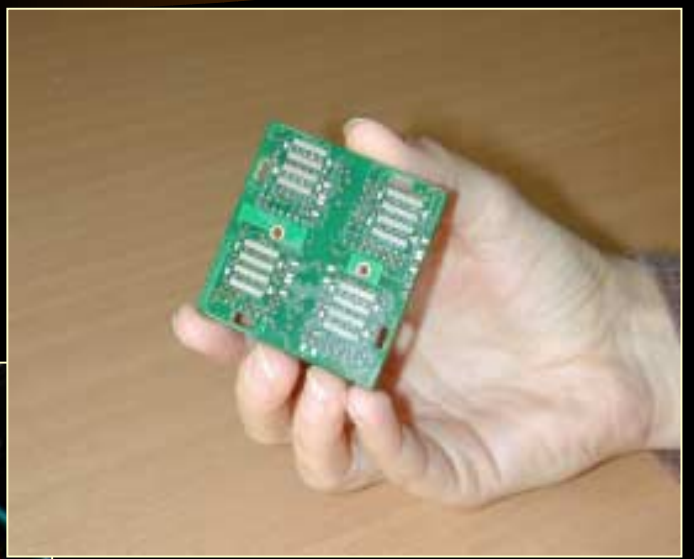
- To match the speed and power consumption requirements, radiation tolerance, compactness and modularity, it is mandatory to build a dedicated ASIC
  - No existing chip (to our knowledge) seems to meet all EUSO requirements
- CMOS sub-µm technologies provide very low power consumption, are fast enough and are almost "naturally" radiation tolerant.
  - Two technologies identified (see www.ge.infn.it/euso/fee.html)
    - **AMS 0.35 mm**, available through EuroPractice
    - **IBM 0.25 mm**, available through RAL

ASIC physical position

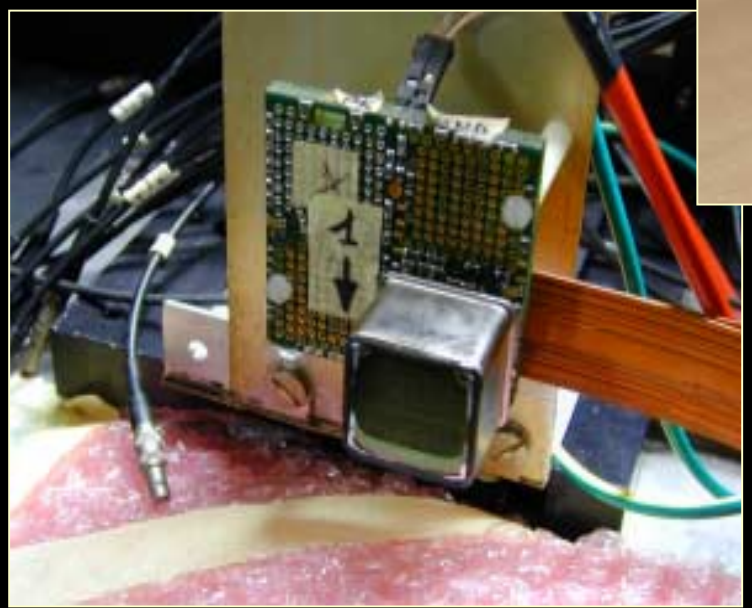
Micro-cell



PCB with voltage dividers, 4 ASICs and other Front End devices



4 pmts per micro cell (256 pixels)



First 2x2 prototype developed and built

Pre-Phase A activity in Genova

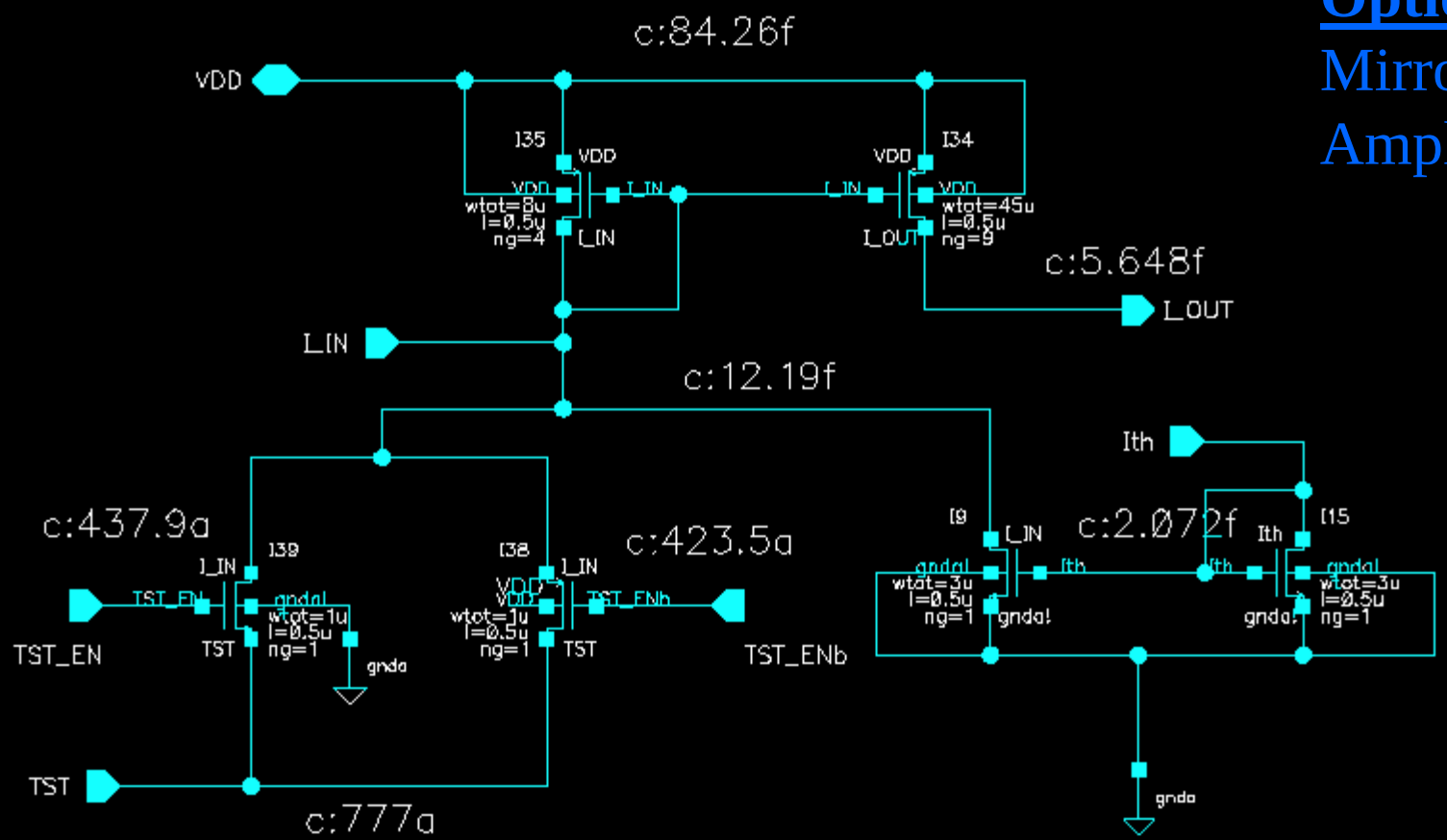
- INFN has approved and funded an RD project whose goal is to prove the feasibility of this approach.
  - Project started in September 2000
  - Many possible **pre-amplifiers** and **comparators** have been **designed and simulated**
  - A test chip has been designed and built (submitted on June 6th, 25 pieces delivered to Genova on september 5th)
    - AMS 0.35 mm through EuroPractice
  - PCB for chip test has been designed and submitted for fabrication.

The "prototype 0" chip

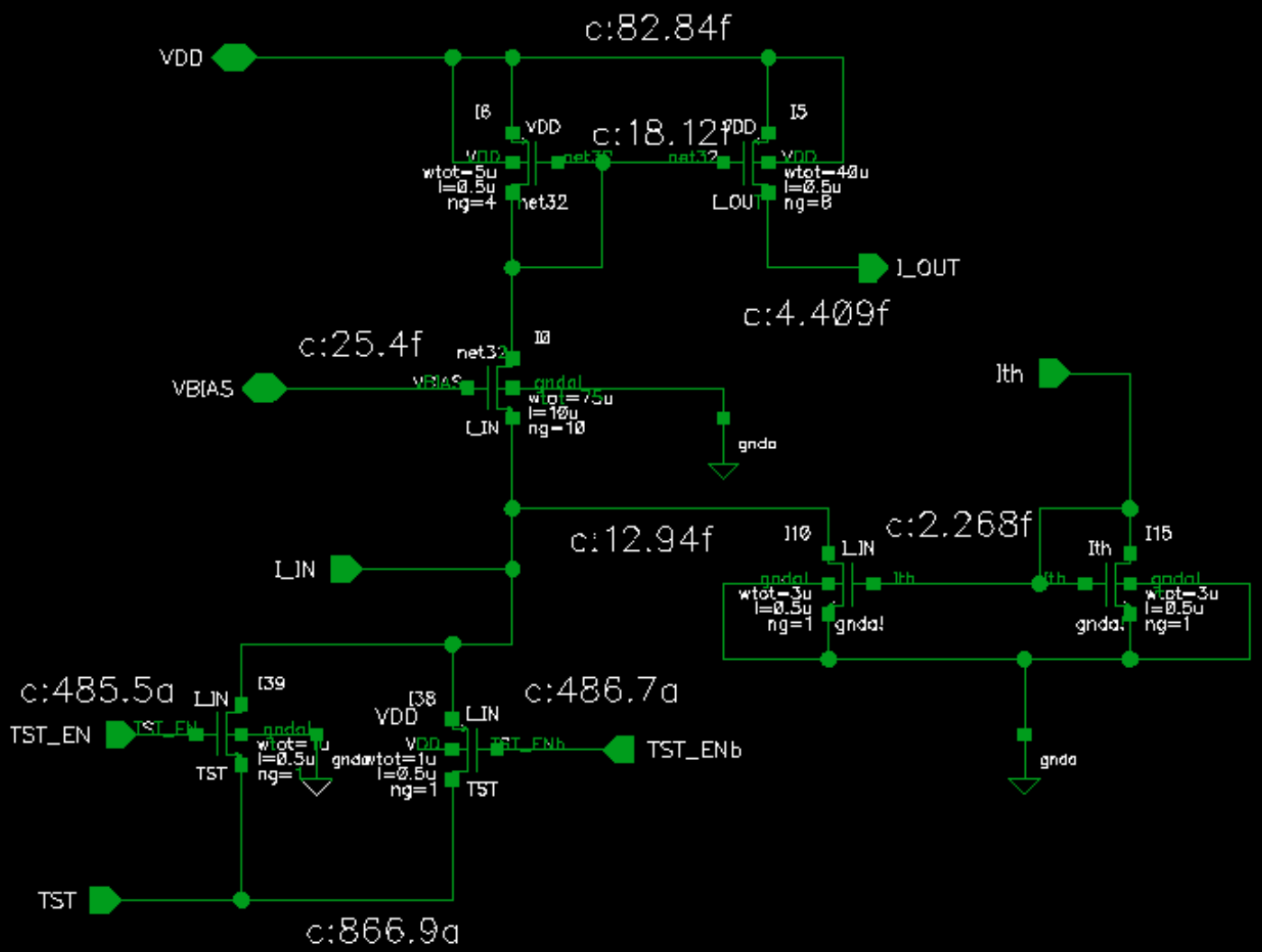
- We have designed and built a simple ASIC to prove the feasibility of the EUSO front end
- This chip contains:
  - 3 different pre-amplifier designs (Options I, II, III)
  - 3 different comparators (Options A,B,C)
  - All 9 combinations of the above
  - DAC for threshold control
  - A minimal digital section to control DACs
- Chip layout allows testing of all options and of the individual elements (pre-amplifier and comparators)

Pre-Amplifier design (I)

Option I
Mirror
Amplifier

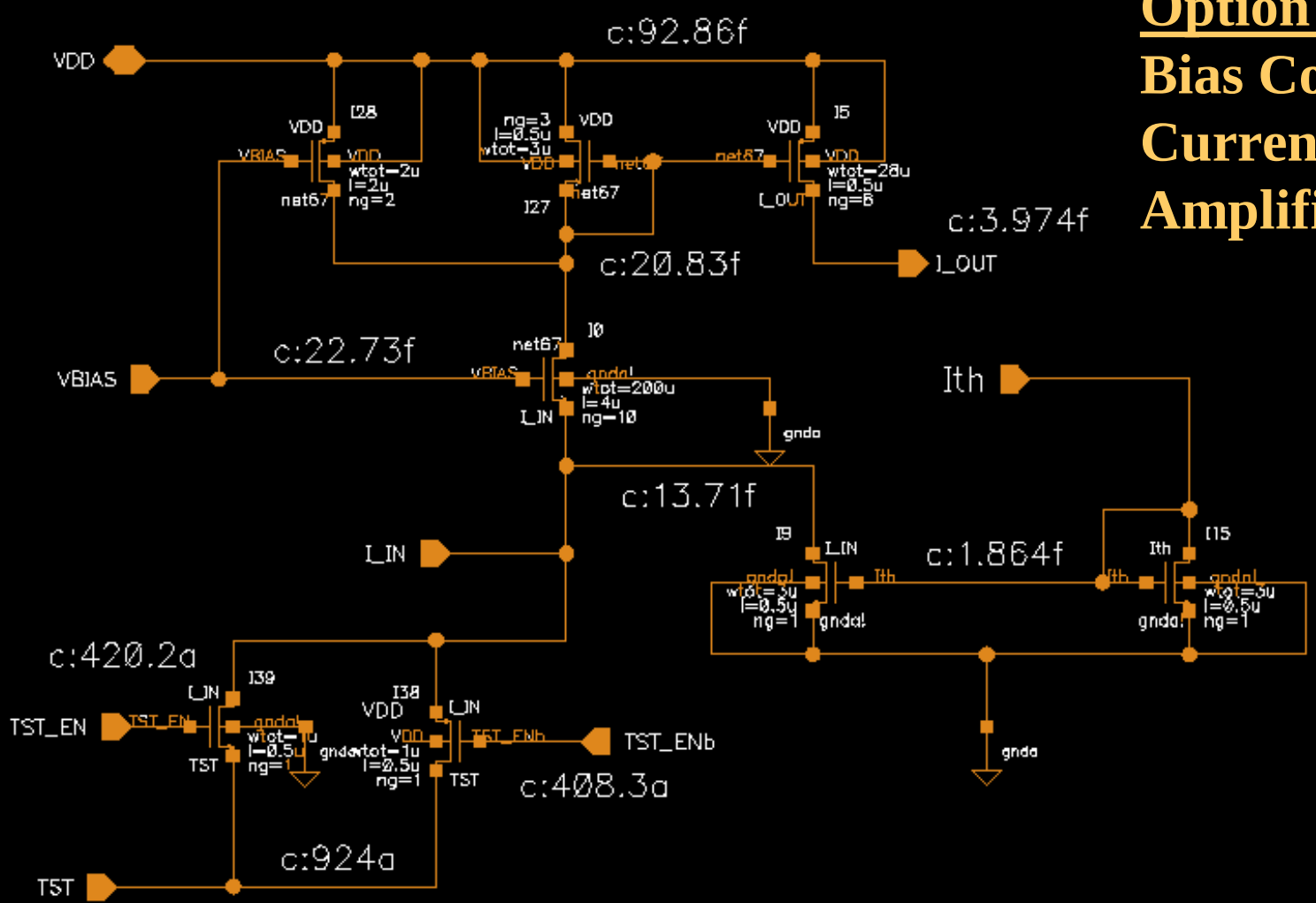


Pre-Amplifier design (II)



Option II
Current Mirror Amplifier

Pre-Amplifier design (III)



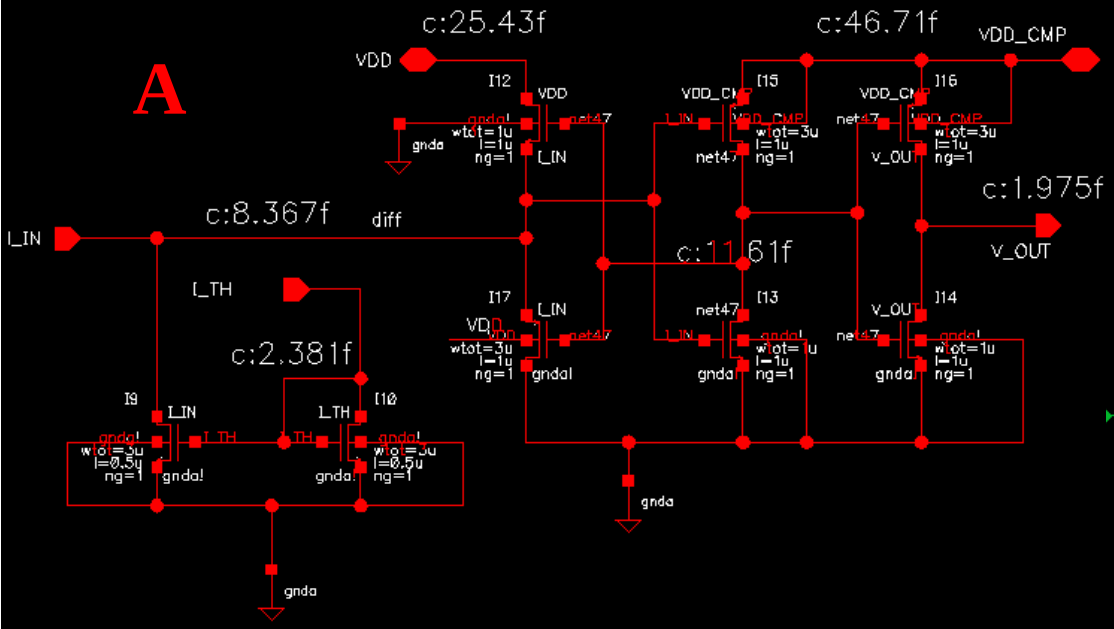
Option III

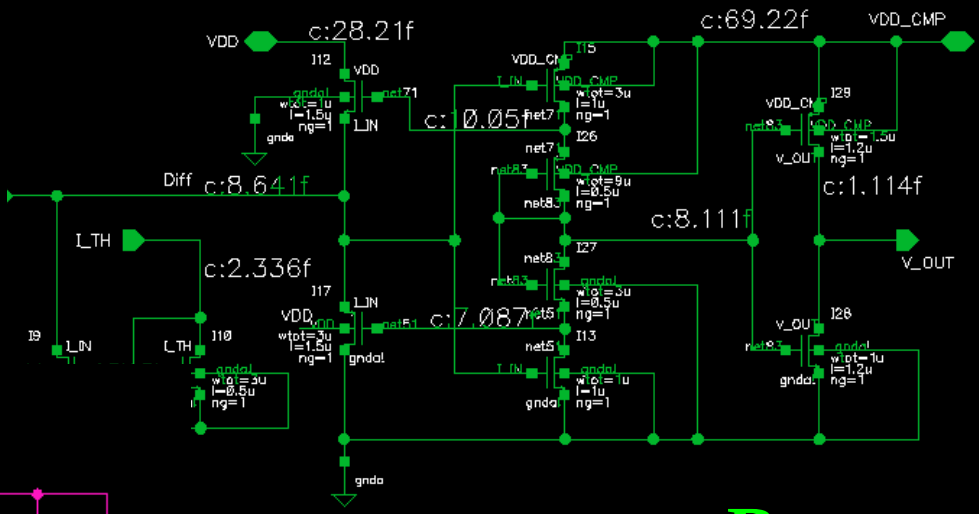
Bias Compensation

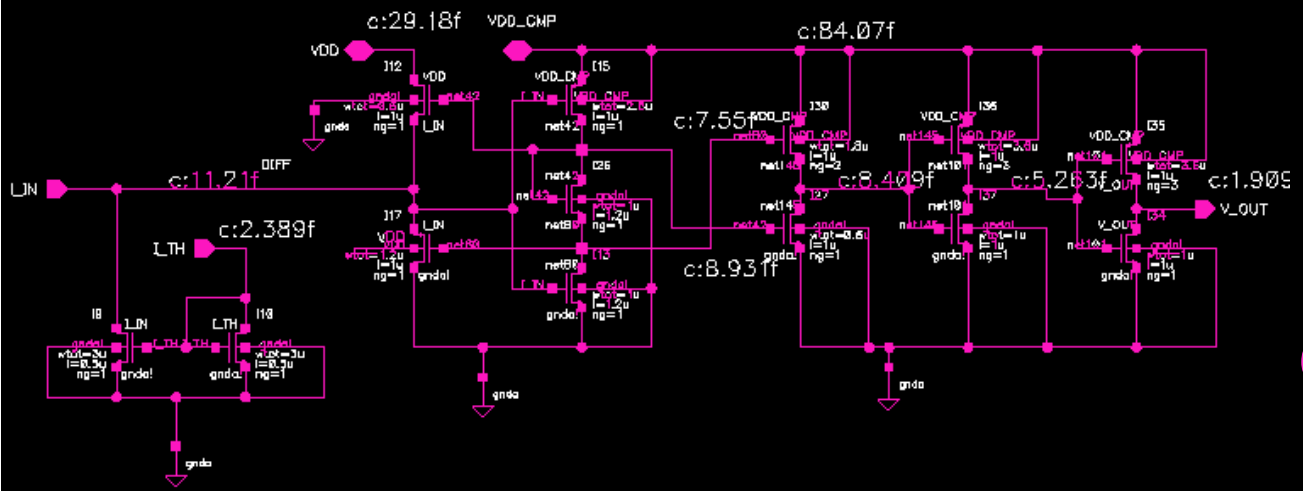
Current Mirror

Amplifier

Discriminator design (I-II-III)







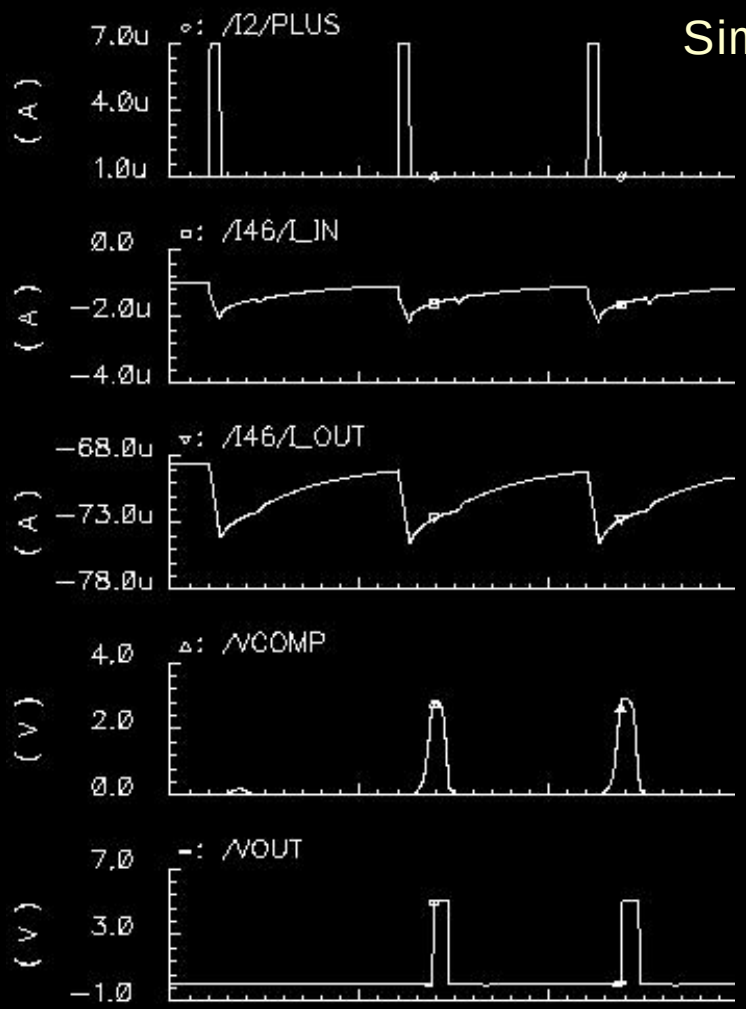
Test chip simulations: power

- Full simulations have been performed to compute power consumption and double hit resolutions
- So far, major effort has been devoted to keep power requirements well within the 1 mW/ch limit (i.e. no power, no Euso!)

DESIGN	I_{th} (μA)	<I> (μA)	<P> (μW)	Width. (ns)
CMA2+ COMPA-A	97.0	260	780	16.1
CMA2+ COMPA-B	98.0	332	996	18.8
MA2+ COMPA-A	71.5	210	630	13.3
MA2+ COMPA-B	71.5	286	858	22.2
BCMA2+ COMPA-A	32.5	129	387	16.6
BCMA2+ COMPA-B	33.0	187	561	17.4
BCMA2+ COMPA-C	33.0	142	426	11.7

Speed

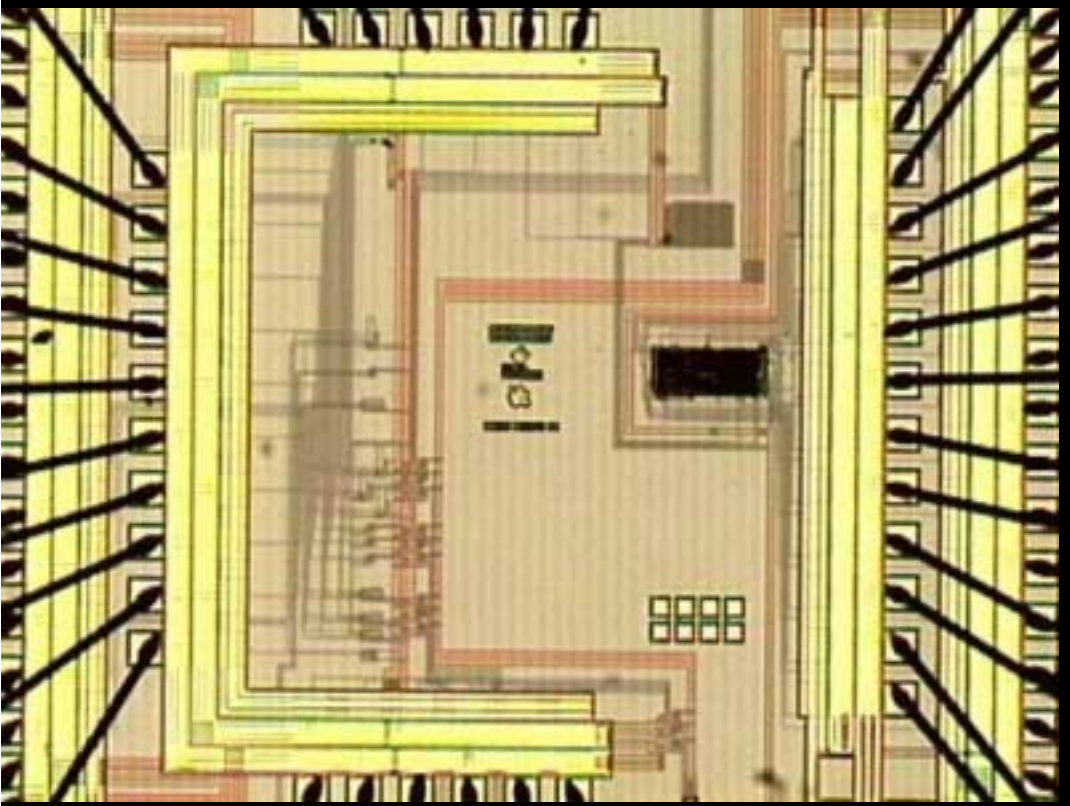
Simulation at 1 MHz



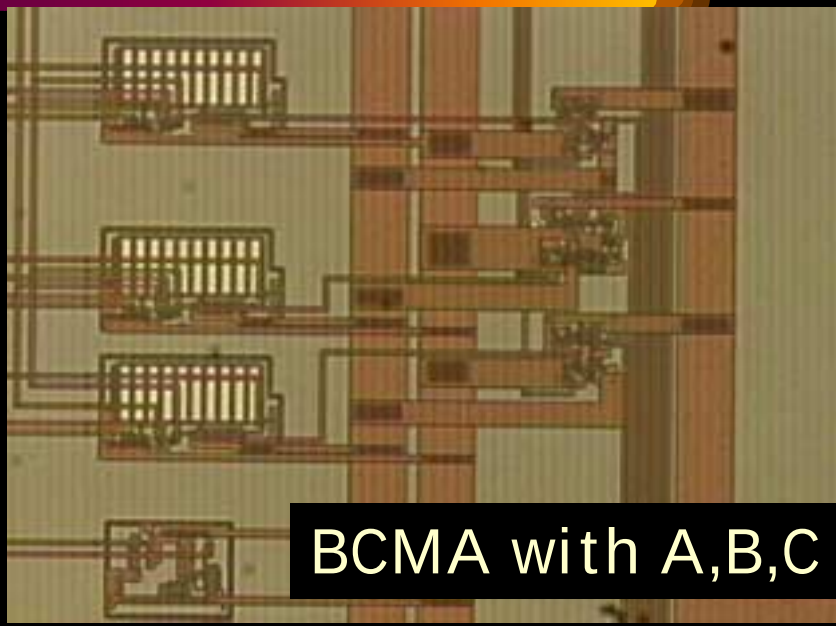
Double hit resolution ≈ 20 ns, depending on design and threshold

Substantial improvement possible, increasing the power consumption

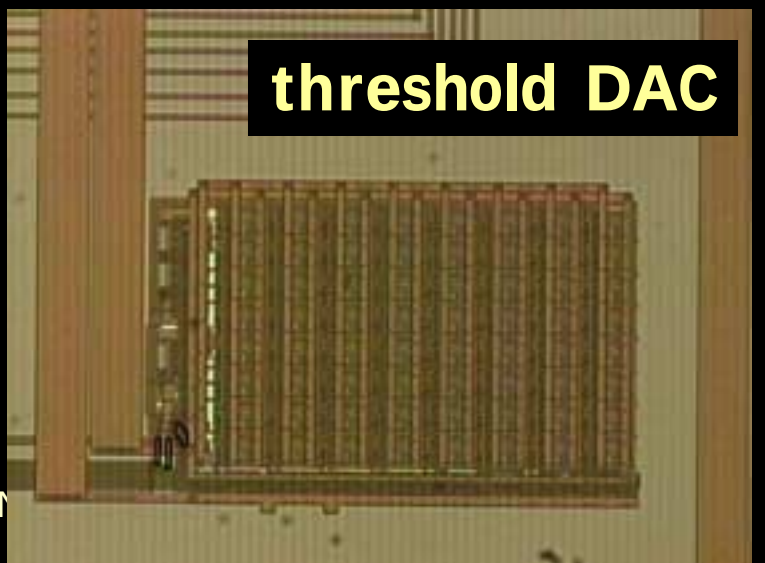
Prototype 0: pictures



whole chip layout

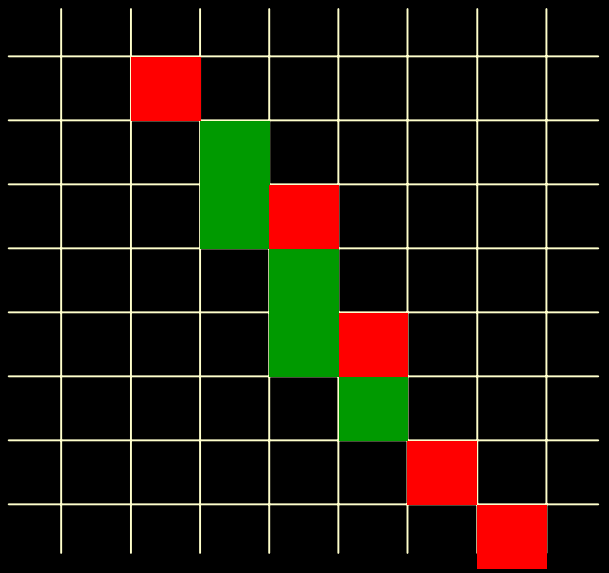


BCMA with A,B,C



threshold DAC

Problem: full recovery of light



No or 1 hit in one GTU

Below counter threshold

Above counter Thr.

- Euso trigger is done in the macrocell electronics using the fast-OR signals gated by the on-chip counters.
- Only the green pixels are read by the system. The photons in the red boxes are lost, degrading both the energy and the angle resolution

Counters Readout (I)

- At each GTU we can store these counters, a digital picture of the atmosphere with 1 μs integration time, in an internal memory, deep enough to wait for the main trigger to occur.
  - 200 GTUs require 200 x 64 x 10 bits = 16 Kbytes
- The MacroCell electronics can read this memory when the main trigger occurs (for all relevant chips)
  - With 1 Mhz serial line, 16 ms read-out time
  - Acceptable ?? Strongly depends on trigger rate!

Counters Readout (II)

- The system could be also useful for slow (atmospheric, metheorites) events
- An additional memory could store the sum of photons gathered in longer periods.
  - If you sum 100 GTUs and use a 16 Kbytes memory you can store the whole information for events as long as 20 ms.

Conclusions

- All pre-phase A activities suggest that a full custom ASIC is required for the front end electronics
- Requirements dictated by physics and space environment have been identified and must be refined and traded off in phase A
- INFN has funded an RD project to develop this device
- A lot of work already done. A study prototype is built. Results will give a final answer to the main question (power vs speed)